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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,712	12/02/2003	Kenneth J. Goodnow	END920030100US1	4333
30449	7590	07/12/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS 3 LEAR JET LANE SUITE 201 LATHAM, NY 12110			DOAN, NGHIA M	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No. 10/725,712	Applicant(s) GOODNOW ET AL.	
	Examiner Nghia M. Doan	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/02/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/02/2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>12/03/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Responsive communication application filed on 12/02/2003, claims 1-30 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because **the abstract contains the language of claim 1 and lacks narrative format**. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 17-30 are objected to because of the following informalities: the preamble should be written as "the computer system" instead of "the system" for correct antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 12 and 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which

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was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The subject "programmable logic device is connectable between an input , output or both of state machine" is not described in specification.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 5 and 20 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Refer to PG Pubs (US 2005/0120323) page 3, ¶ 28, line 3-4, applicant has stated "the FPGA netlist compiled into a SRAM configuration pattern", and this statement indicates that the invention is different from what is defined in the claim(s) because programmable logic device can not be compiled into a pattern. Applicant should revise the claims language for consistent to specification.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Osann, JR. et al. (Osann) (US 2002/0010903).**

10. **With respect to claims 1 and 16, Osann discloses a computer system comprising a processor, an address/data bus coupled to said processor, and a**

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computer readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement (claim 10 – claim 16, -- the computer readable medium and including instructions for performing the step of--) a method for modification function of a state machine have a programmable logic device (abstract), said method comprising implemented step of:

a) modifying a high-level design of said state machine (logic block) to obtain a modified high- level design of said state machine with a modified function (pg. 3, ¶ 39, ll. 5-14);

b) generating a programmable logic device netlist from differences in said high-level design and said modified design (pg. 3, ¶ 48, ll. 1-9; ¶ 52, ll. 3-9); and

(c) installing (loading) said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist (pg. 4, ¶ 52, ll. 3-13).

11. **With respect to claims 2 and 17**, Osann discloses the limitations of claims 1 and 16 respectively, wherein step (b) includes:

extracting a high-level programmable logic device design from said modified high-level design (fig. 9, 10; pg. 3, ¶ 46, ll.1-5).

12. **With respect to claims 3 and 18**, Osann discloses the limitations of claim 2 and 17 respectively, wherein said extracting includes comparing (simulation) said high-level design to said modified high-level design (pg. 3, ¶ 44, ll. 4-15; ¶ 47; and ¶ 48, ll. 5-15).

13. **With respect to claims 4 and 19**, Osann discloses the limitations of claim 2 and 17 respectively, wherein said generating a programmable logic device netlist includes synthesizing said a high-level programmable logic device design (pg. 3, ¶ 47, ll. 1-6).

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14. **With respect to claims 5 and 20**, Osann discloses the limitations of claim 4 and 19 respectively, wherein said programming of said programmable logic device includes compiling (converting) said programmable logic device into a pattern (fig. 10, pg. 4, ¶ 52, ll. 3-12) and applying said pattern to a static random access memory array (fig. 11, 12, two bit-storage units -- unit cell of SRAM -- or programming memory) of an integrated circuit containing said state machine and said programmable logic device (pg. 6, ¶ 83-¶ 84; pg. 7, ¶ 89, ll. 1-9).

15. **With respect to claims 6 and 21**, Osann discloses the limitations of claim 1 and 16 respectively, further including the step of:

(d) determining if said programmable logic device includes enough gates to program said modified function (pg. 3, ¶ 43, and ¶ 44, ll. 9-15).

16. **With respect to claims 7 and 22**, Osann discloses the limitations of claim 1 and 16 respectively, further including, before step (a) performing a static timing analysis (extraction and simulation) to determine a maximum allowable size for said programmable logic device (pg. 3, ¶ 48, ll. 5-15).

17. **With respect to claims 8 and 23**, Osann discloses the limitations of claim 6 and 21 respectively, wherein said performing said static timing analysis is performed on a netlist synthesized from said high-level design of said state machine (pg. 3, ¶ 46, ll. 1-6 and ¶ 48, ll. 5-15).

18. **With respect to claims 9 and 24**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said high-level design of said state machine is a portion of a high level design of an integrated circuit and said modified high-level design of said

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state machine is a portion of a modified version of said high level design of said integrated circuit (pg. 3, ¶ 39, ll. 5-19, ¶ 42, ll. 4-16).

19. **With respect to claims 10 and 25**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said high-level design of said state machine includes one or more multiplexers for interconnecting said programmable logic device to said state machine (fig. 11, 12, and 17 and pg. 4, ¶ 59, ll. 1-8).

20. **With respect to claims 11 and 26**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said programmable logic device is connectable between a next stage logic and a state latch of said state machine in either a next state path, a current state path or both (fig. 13, 13a, 14 and 14a; and pg. 5, ¶ 74-¶ 76).

21. **With respect to claims 12 and 27**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said programmable logic device (PLA) is connectable between an input (I) of said state machine, an output of said state machine or both (Z, X, Y) (fig. 7, pg. 3, ¶ 40, ll. 1-13).

22. **With respect to claims 13 and 28**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said programmable logic device is adapted to add programmable logic device latch bits (bit-storage) to a state latch of said state machine (pg. 4, ¶ 56, ll. 1-7; ¶ 57, ll. 1-17; and pg. 5, ¶ 74, ll. 1-15).

23. **With respect to claims 14 and 29**, Osann discloses the limitations of claim 1 and 16 respectively, wherein said programmable logic device is shared between said state machine and one or more additional state machines (PLA) (fig. 3 and 8; pg. 1, ¶ 9, 1-12; pg. 3, ¶ 40, ll. 8-13 and ¶ 43, ll. 1-9)

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24. With respect to claims 15 and 30, Osann discloses the limitations of claim 1 and 16 respectively, wherein said programmable logic device is selected from the group consisting of programmable logic arrays (PLA) (fig. 1-3 and pg. 4, ¶ 54-56)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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